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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant Andrew Marshall Docket Number: TI-34177

Serial No.: 10/626,438 Art Unit: 2818

Filed: 07/24/03 Examiner: Thong Quoc Le

For: Circuit for Reducing Standby Leakage in a Memory Unit

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below:

Karen Vertz
Karen Vertz

4-14-05
Date

FACSIMILE COVER SHEET

X FACSIMILE COVER SHEET	X AMENDMENT 111 (6 pages)
___ NEW APPLICATION	___ EOT
___ DECLARATION	___ NOTICE OF APPEAL
___ ASSIGNMENT	___ APPEAL (# Pages)
___ FORMAL DRAWINGS	___ ISSUE FEE & PUBLICATION FEE (1 Page)
X INFORMAL DRAWINGS – 1 page	___ REPLY BRIEF (IN TRIPLICATE) (# Pages)
___ CONTINUATION APP'N	___ ELECTION
___ DIVISIONAL APP'N	

NAME OF INVENTOR(S): Andrew Marshall	RECEIPT DATE & SERIAL NO.: Serial No.: **10/626,438** Filing Date: 07/24/03
TITLE OF INVENTION: Circuit for Reducing Standby Leakage in a Memory Unit	
TI FILE NO.: TI-34177 / DEPOSIT ACCT. NO.: 20-0668	
FAXED: 4-14-05 DUE: 4-14-05 ATTY/SEC'Y: AKS/klv	

Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, TX 75265-5474

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Andrew Marshall **Art Unit: 2818**

Serial No.: 10/626,438 **Examiner: Thong Quoc Le**

Filed: 07/24/03 **Docket: TI-34177**

For: CIRCUIT FOR REDUCING STANDBY LEAKAGE IN A MEMORY UNIT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CERTIFICATION OF FASCIMILE TRANSMISSION
I hereby certify that the above correspondence is being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9306 on the date shown below:

Karen Vertz 4-14-05
Karen Vertz Date

AMENDMENT

In response to the Official Action in this case mailed January 14, 2005, please enter the following:

IN THE CLAIMS

1. (Currently amended) A circuit for reducing standby leakage in a memory unit, comprising:
a capacitive divider coupled to the memory unit so as to generate a voltage across the memory unit, the voltage being adequate to retain memory values during one of a sleep state and a standby state, wherein the memory unit is coupled between Vss and Vddinternal terminals.

2. (Original) The circuit according to claim 1, wherein said capacitive divider is coupled to the memory unit on-chip.

3. (Original) The circuit according to claim 1, wherein the voltage is a division of a normal operating voltage.

4. (Original) The circuit according to claim 3, wherein the voltage is substantially Vdd/2.

5. (Original) The circuit according to claim 3, wherein the voltage is substantially Vdd/3.

6. (Original) The circuit according to claim 1, wherein said capacitive divider is configured for varying an oscillator frequency in accordance with the generated voltage so as to minimize switching losses.

7-10. (Cancelled)

11. (Currently amended) An inductive circuit for reducing standby leakage in a memory unit, comprising:
an inductive divider coupled to the memory unit so as to generate a voltage across the memory unit, the voltage being adequate to retain memory values during one of a sleep state and a standby state, wherein the memory unit is coupled between Vss and Vddinternal terminals.

12. (Original) The inductive circuit according to claim 11, wherein said inductive divider is coupled to the memory unit on-chip.

13. (Original) The inductive circuit according to claim 11, wherein the voltage is a division of a normal operating voltage.

14. (Original) The inductive circuit according to claim 13, wherein the voltage is substantially Vdd/2.

15. (Original) The inductive circuit according to claim 13, wherein the voltage is substantially Vdd/3.

16. (Original) The inductive circuit according to claim 11, wherein said inductive divider is configured for varying an oscillator frequency in accordance with the generated voltage so as to minimize switching losses.

17-20. (Cancelled)

REMARKS

Claims 1-20 are pending in the application. Claims 1-6, 8-16 and 18-20 are rejected. Claims 7 and 17 are objected to. Claims 1 and 11 have been amended. Claims 7-10 and 17-20 have been cancelled.

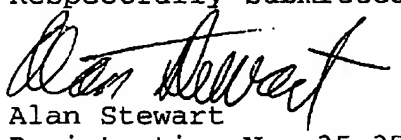
The drawings were objected to. A drawing replacement sheet is attached that adds the legend "Prior Art" to Figure 1 and adds the labels 200, 202, and 204 to Figure 2.

The drawings were objected to because the drawings must show every feature of the invention specified in the claims. This has been corrected by canceling Claims 8, 9, 18, and 19.

Claim 1 has been amended to include the limitations of objected claim 7. Claims 2-6 depend from claim 1. Claim 11 has been amended to include the limitations of objected claim 17. Claims 12-16 depend from claim 11. Therefore, claims 1-6 and 11-16 are believed to be allowable.

It is believed that the above remarks and amendments are fully responsive to the Official Action. Reconsideration and allowance are therefore respectfully requested.

Respectfully submitted,



Alan Stewart
Registration No. 35,373

Texas Instruments, Incorporated
P. O. Box 655474 - M/S 3999
Patent Department
Dallas, Texas 75265

Replacement Sheet

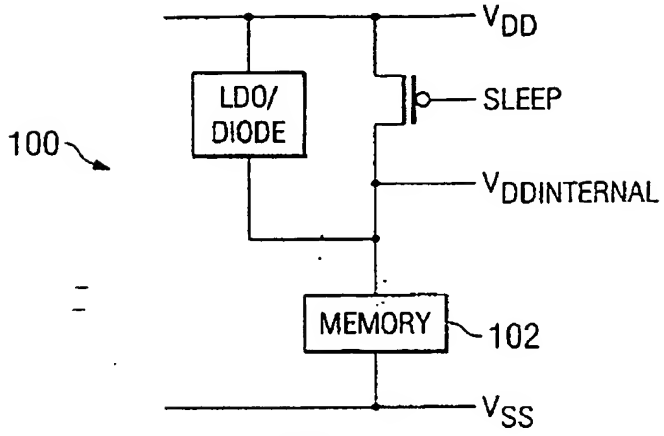


FIG. 1
(Prior Art)

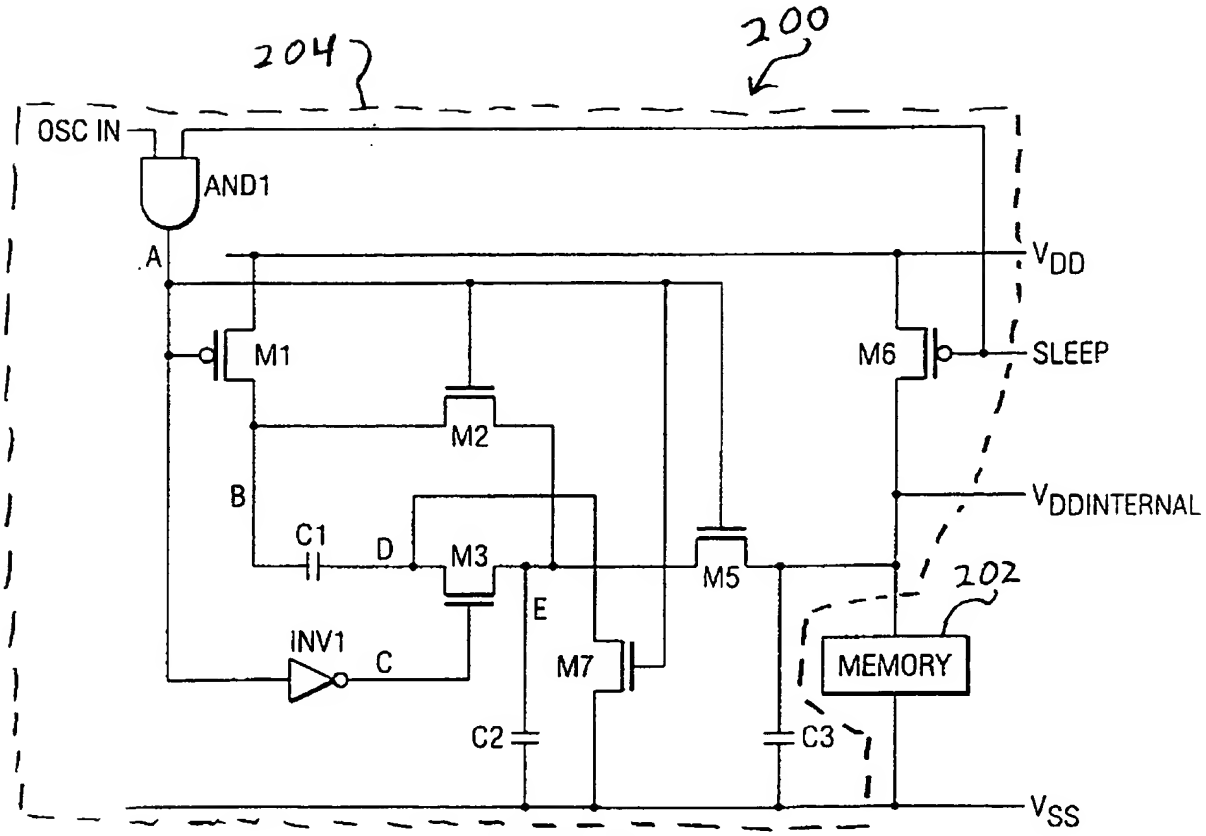


FIG. 2